IN THE CLAIMS:

Rewrite the pending claims as follows:

1. (Currently Amended) A slave device for use in a master-slave system, comprising:

a clock node to receive an externally-provided clock signal;

a phase-to-master node to receive a phase-to-master phase signal; and

a phase-from-master node to receive a phase-from-master phase signal;

wherein the externally-provided clock signal, the phase-to-master phase signal and the phase-from-master phase signal are distinct signals received at distinct nodes of the slave device; and

wherein said slave device includes a delay-locked loop configured to process said clock signal and said phase-to-master signal to produce a transmit clock signal.

2. (canceled)

3. (Currently Amended) The slave device of claim 1 ~~2~~ wherein said slave device includes transmit circuitry to transmit data to a data bus in response to said transmit clock signal.

4. (Previously presented) The slave device of claim 1 wherein said slave device includes a delay-locked loop configured to process said externally-provided clock signal and said phase-from-master signal to produce a receive clock signal.

5. (Previously presented) The slave device of claim 4 wherein said slave device includes receive circuitry configured to receive data from a data bus in response to said receive clock signal.

6. (Previously presented) The slave device of claim 1 wherein said slave device is configured to process a single-ended phase-to-master phase signal.

7. (Previously presented) The slave device of claim 1 wherein said slave device is configured to process a single-ended phase-from-master phase signal.

8. (Currently amended) A master-slave system, comprising:

a clock signal generator configured to produce a clock signal;

a phase signal generator configured to produce a phase signal;

a clock line connected to said clock signal generator to carry said clock signal;

a phase line connected to said phase signal generator to carry said phase signal, said phase line including a phase-to-master path to carry a phase-to-master phase signal and a phase-from-master path to carry a phase-from-master phase signal;

a master device connected to said clock line and said phase line;

a data bus connected to said master device; and

a slave device connected to said data bus, said clock line and said phase line, said slave device configured to process data on said data bus in response to said clock signal, said phase-from-master phase signal and said phase-to-master phase signal;

wherein said phase signal has an effective frequency that is lower than a frequency of said clock signal.

9. (Currently amended) The master-slave system of claim 8 wherein said phase signal generator includes a divide-by-N effective-frequency circuit to produce said phase signal from said clock signal.

10. (Previously presented) The master-slave system of claim 8 wherein said phase signal generator includes a pseudo-random number generator to produce said phase signal from said clock signal.

11. (Currently Amended) The master-slave system of claim 8 wherein said slave device includes a delay-locked loop to process said clock signal and said phase-to-master phase signal to produce a transmit clock signal.

12. (Previously presented) The master-slave system of claim 11 wherein said slave device includes transmit circuitry to transmit data to said data bus in response to said transmit clock signal.

13. (Currently Amended) The master-slave system of claim 8 wherein said slave device includes a delay-locked loop to process said clock signal and said phase-from-master phase signal to produce a receive clock signal.

14. (Previously presented) The master-slave system of claim 13 wherein said slave device includes receive circuitry to receive data from said data bus in response to said receive clock signal.

15. (Canceled)

16. (Previously presented) The master-slave system of claim 8 wherein said phase signal is non-periodic.

17. (Currently amended) A method of operating a master-slave system, said method comprising:

generating a clock signal and a phase signal, said phase signal including a phase-to-master signal and a phase-from-master signal;

at an interface of a slave device, receiving said clock signal, said phase-from-master signal and said phase-to-master signal;

at the slave device, transmitting data to a master device in response to said clock signal and said phase-to-master signal; ~~and~~

at the slave device, receiving data from said master device in response to said clock signal and said phase-from-master signal; and

producing a receive clock signal having a frequency determined by said clock signal and a phase determined by said phase-from master signal.

18. (Currently Amended) The method of claim 17 wherein said transmitting data comprises:

producing a transmit clock signal having a frequency ~~and a phase determined~~ by said clock signal and a phase determined by said phase-to-master signal.

19. (original) The method of claim 18 wherein said transmitting data comprises:

operating data transmit circuitry in response to said transmit clock signal.

20. (canceled)

21. (Currently Amended) The method of claim 17 ~~20~~ wherein said receiving data comprises:

operating receive circuitry in response to said receive clock signal.

22. (Previously presented) The method of claim 17 wherein said generating includes generating said phase signal from said clock signal.

23. (Currently Amended) The method of claim 22 wherein said generating includes generating said phase signal as [[a]] an effective-frequency-divided clock signal.

24. (Previously presented) The method of claim 22 wherein said generating includes generating said phase signal as a pseudo-random function of said clock signal.

25. (Currently Amended) The method of claim 17 [22] wherein said phase signal has an effective frequency that is lower than the frequency of said clock signal.

26. (original) The method of claim 22 wherein said phase signal is non-periodic.

27. (Previously presented) The method of claim 17 wherein said phase signal is non-periodic.

28. (Previously presented) The method of claim 17, wherein said master device is a memory controller and said slave device is a memory device.

29. (Currently Amended) The slave device of claim 1, wherein said phase-to-master signal and said phase-from-master signal each have an effective frequency that is lower than [the] a frequency of said clock signal.

30. (Previously presented) The slave device of claim 1, wherein said slave device is an integrated circuit device.

31. (Previously presented) The integrated circuit device of claim 1, wherein said slave device is a memory device.

32. (Previously presented) The master-slave system of claim 8, wherein said master device is a memory controller and said slave device is a memory device.

33. (New) A device for use in a system, comprising:

a clock node to receive an externally-provided clock signal;

a first node to receive an externally-provided first phase signal; and

a second node to receive an externally-provided second phase signal;

wherein the externally-provided clock signal, the first phase signal and the second phase signal are distinct signals received at distinct nodes of the slave device; and

wherein the first phase signal and the second phase signal each have an effective frequency that is lower than a frequency of the clock signal.

34. (New) A system, comprising:

a clock signal generator configured to produce a clock signal;

a phase signal generator configured to produce a phase signal;

a clock line connected to said clock signal generator to carry said clock signal;

a phase line connected to said phase signal generator to carry said phase signal, said phase line including a first path to carry a first phase signal and a second path to carry a second phase signal;

a first device connected to said clock line and said phase line;

a data bus connected to said first device; and

a second device connected to said data bus, said clock line and said phase line, said second device configured to process data on said data bus in response to said clock signal, said first phase signal and said second phase signal;

wherein said second device includes a delay-locked loop to process said clock signal and said first phase signal to produce a transmit clock signal.

35. (New) A method of operating a system having a first device and a second device, said method comprising:

generating a clock signal and a phase signal, said phase signal including a first phase signal and a second phase signal;

at an interface of the second device, receiving said clock signal, said first phase signal and said second phase signal;

at the second device, transmitting data to the first device in response to said clock signal and said first phase signal;

at the second device, receiving data from the first device in response to said clock signal and said second phase signal; and

producing a receive clock signal having a frequency determined by said clock signal and a phase determined by said second phase signal;

wherein said first phase signal and said second phase signal each have an effective frequency that is lower than a frequency of said clock signal.